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EXAMINER	
ORTIZ, EDGARDO	
ART UNIT	**PAPER NUMBER**
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/927,320	Applicant(s) Darwish Et.al.
	Examiner Edgardo Ortiz	Art Unit 2815

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) [X] Responsive to communication(s) filed on *Oct 14, 2003* .

2a) [X] This action is **FINAL**. 2b) [ ] This action is non-final.

3) [ ] Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) [X] Claim(s) *2-8, 10-14, 16, 18, 30, and 31* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) [ ] Claim(s) _____ is/are allowed.

6) [X] Claim(s) *2-8, 10-14, 16, 18, 30, and 31* is/are rejected.

7) [ ] Claim(s) _____ is/are objected to.

8) [ ] Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) [ ] The specification is objected to by the Examiner.

10) [ ] The drawing(s) filed on _____ is/are a) [ ] accepted or b) [ ] objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) [ ] The proposed drawing correction filed on _____ is: a) [ ] approved b) [ ] disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) [ ] The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) [ ] Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) [ ] All b) [ ] Some* c) [ ] None of:

1. [ ] Certified copies of the priority documents have been received.
2. [ ] Certified copies of the priority documents have been received in Application No. _____ .
3. [ ] Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) [ ] Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) [ ] The translation of the foreign language provisional application has been received.

15) [ ] Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) [X] Notice of References Cited (PTO-892)
2) [ ] Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) [ ] Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) [ ] Interview Summary (PTO-413) Paper No(s). _____
5) [ ] Notice of Informal Patent Application (PTO-152)
6) [ ] Other:

DETAILED ACTION

This Office Action is in response to an amendment filed October 14, 2003 in which Applicant amended claims 4, 11, 16 and 18 and canceled claims 1, 9, 15, 17 and 19-29.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-8, 10-14, 16, 18, 30 and 31 are rejected under 35 U.S.C.§ 103 (a) as being unpatentable over Hshieh (U.S. Patent No. 6,262,543) in view of Blanchard (U.S. Patent No. 4,893,160). With regard to Claim 2, Hshieh teaches a gate (125) adjacent to a first insulative layer (120) and a second insulative layer (120') within said trench.

With regard to Claim 3, Hshieh teaches a gate (125) that comprises polysilicon.

With regard to Claim 4, Hshieh teaches a semiconductor substrate, which includes layers (105, 110, 130, 138, 160), defining a trench extending into said substrate from a surface of said substrate, a source region (140) of a first conductivity type (n) adjacent to a sidewall of said trench and to said surface, a body region (130) of a second conductivity type (p) opposite to said

first conductivity type, adjacent to said source region and to said sidewall, a drain region comprising the epitaxial layer (110), of said first conductivity type adjacent to said body region and to said sidewall, wherein said trench is lined with a first insulative layer (120) along a portion of said sidewall that abuts said body region and wherein said trench with a second insulative layer (120') along said bottom portion of said trench, said second insulative layer being in contact with said first insulative layer and a highly doped region (118) of said first conductivity in a drain region (110) adjacent to at least said bottom portion of a trench.

However, Hshieh fails to teach that the highly doped region is in contact with the bottom of the trench. Blanchard discloses a semiconductor trenched device which includes an epitaxial region (12), a trench (36) and a highly doped region (39) which surrounds and is in contact with the bottom of the trench (36). Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Hshieh to include a highly doped region that is in contact with the bottom of the trench, as clearly suggested by Blanchard, in order to achieve higher breakdown voltage (see column 2, lines 48-51).

The limitation "second *deposited* insulative layer" is a product by process limitation. A "product by process" claim is directed to the product per se, no matter how actually made, In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186

USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. Furthermore, the generic term "*deposited*", used to describe the second insulative layer, is met by the reference.

Additionally, the limitation "*whereby formation of said second insulative layer does not introduce substantial stress in said substrate*" is an intended use limitation which does not structurally distinguish the claimed invention from that taught by the teachings of Hshieh.

With regard to Claim 5, Hshieh teaches a first insulative layer (120) comprising an oxide.

With regard to Claim 6, Hshieh teaches a second insulative layer (120') comprising an oxide.

With regard to Claim 7, Hshieh teaches a second insulative layer (120') is a multi-layer insulative layer, comprising dry oxidation grown oxide layers.

With regard to Claim 8, Hshieh teaches an MIS device that is a MOSFET.

With regard to Claim 10, Hshieh teaches a gate (125) that comprises polysilicon.

With regard to Claim 11, Hshieh teaches a semiconductor substrate, which includes layers (105, 110, 130, 138, 160), defining a trench extending into said substrate from a surface of said substrate, a source region (140) of a first conductivity type (n) adjacent to a sidewall of said trench and to said surface, a body region (130) of a second conductivity type (p) opposite to said first conductivity type, adjacent to said source region and to said sidewall, a drain region comprising the epitaxial layer (110), of said first conductivity type adjacent to said body region and to said sidewall, wherein said trench is lined with a first insulative layer (120) along a portion of said sidewall that abuts said body region and wherein said trench with a second insulative layer (120') along said bottom portion of said trench, said second insulative layer being in contact with said first insulative layer and said second insulative layer being thicker than said first insulative layer, a gate (125) adjacent to said first insulative layer (120) and said second insulative layer (120') within said trench and a highly doped region (118) of said first conductivity in a drain region (110) adjacent to at least said bottom portion of a trench.

However, Hshieh fails to teach that the highly doped region is in contact with the bottom of the trench. Blanchard discloses a semiconductor trenched device which includes an epitaxial region

(12), a trench (36) and a highly doped region (39) which surrounds and is in contact with the bottom of the trench (36). Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Hshieh to include a highly doped region that is in contact with the bottom of the trench, as clearly suggested by Blanchard, in order to achieve higher breakdown voltage (see column 2, lines 48-51).

The limitation "second *deposited* insulative layer" is a product by process limitation. A "product by process" claim is directed to the product per se, no matter how actually made, In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. Furthermore, the generic term "*deposited*", used to describe the second insulative layer, is met by the reference.

Additionally, the limitation "*whereby formation of said second insulative layer does not introduce substantial stress in said substrate*" is an intended use limitation which does not structurally distinguish the claimed invention from that taught by the teachings of Hshieh.

With regard to Claim 12, Hshieh teaches a first insulative layer (120) comprising an oxide.

With regard to Claim 13, Hshieh teaches a second insulative layer (120') comprising an oxide.

With regard to Claim 14, Hshieh teaches a second insulative layer (120') comprising a multi-layer insulative layer, comprising dry oxidation grown oxide layers.

With regard to Claim 16, Hshieh teaches a semiconductor substrate, which includes layers (105, 110, 130, 138, 160), defining a trench extending into said substrate from a surface of said substrate, a source region (140) of a first conductivity type (n) adjacent to a sidewall of said trench and to said surface, a body region (130) of a second conductivity type (p) opposite to said first conductivity type, adjacent to said source region and to said sidewall, a drain region comprising the epitaxial layer (110), of said first conductivity type adjacent to said body region and to said sidewall, wherein said trench is lined with a first insulative layer (120) along a portion of said sidewall that abuts said body region and wherein said trench with a second insulative layer (120') along said bottom portion of said trench, said second insulative layer being

in contact with said first insulative layer and said second insulative layer being thicker than said first insulative layer, wherein a thickness of a transition insulative layer at the juncture of said first insulative layer and said second insulative layer is not less than a thickness of said first insulative layer, a gate (125) adjacent to said first insulative layer (120) and said second insulative layer (120') within said trench and a highly doped region (118) of said first conductivity in a drain region (110) adjacent to at least said bottom portion of the trench.

However, Hshieh fails to teach that the highly doped region is in contact with the bottom of the trench. Blanchard discloses a semiconductor trenched device which includes an epitaxial region (12), a trench (36) and a highly doped region (39) which surrounds and is in contact with the bottom of the trench (36). Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Hshieh to include a highly doped region that is in contact with the bottom of the trench, as clearly suggested by Blanchard, in order to achieve higher breakdown voltage (see column 2, lines 48-51).

The limitation "second *deposited* insulative layer" is a product by process limitation. A "product by process" claim is directed to the product per se, no matter how actually made, In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re

Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. Furthermore, the generic term "*deposited*", used to describe the second insulative layer, is met by the reference.

Additionally, the limitation "*whereby formation of said second insulative layer does not introduce substantial stress in said substrate*" is an intended use limitation which does not structurally distinguish the claimed invention from that taught by the teachings of Hshieh.

With regard to Claim 18, Hshieh teaches a semiconductor substrate, which includes layers (105, 110, 130, 138, 160), defining a trench extending into said substrate from a surface of said substrate, a source region (140) of a first conductivity type (n) adjacent to a sidewall of said trench and to said surface, a body region (130) of a second conductivity type (p) opposite to said first conductivity type, adjacent to said source region and to said sidewall, a drain region comprising the epitaxial layer (110), of said first conductivity type adjacent to said body region and to said sidewall, wherein said trench is lined with a first insulative layer (120) along a portion of said sidewall that abuts said body region and wherein said trench with a second

insulative layer (120') along said bottom portion of said trench, said second insulative layer being in contact with said first insulative layer and said second insulative layer being thicker than said first insulative layer, wherein a width of said trench at a vertical midpoint of said second insulative layer is not greater than a width of said trench adjacent to said body region, a gate (125) adjacent to said first insulative layer (120) and said second insulative layer (120') within said trench and a highly doped region (118) of said first conductivity in a drain region (110) adjacent to at least said bottom portion of the trench.

However, Hshieh fails to teach that the highly doped region is in contact with the bottom of the trench. Blanchard discloses a semiconductor trenched device which includes an epitaxial region (12), a trench (36) and a highly doped region (39) which surrounds and is in contact with the bottom of the trench (36). Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Hshieh to include a highly doped region that is in contact with the bottom of the trench, as clearly suggested by Blanchard, in order to achieve higher breakdown voltage (see column 2, lines 48-51).

The limitation "second *deposited* insulative layer" is a product by process limitation. A "product by process" claim is directed to the product per se, no matter how actually made, In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186

USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. Furthermore, the generic term "*deposited*", used to describe the second insulative layer, is met by the reference.

Additionally, the limitation "*whereby formation of said second insulative layer does not introduce substantial stress in said substrate*" is an intended use limitation which does not structurally distinguish the claimed invention from that taught by the teachings of Hshieh.

With regard to Claims 30 and 31, the limitation "*the first insulative is thermally grown*" is a product by process claim which does not structurally distinguish the claimed from that taught by Hshieh. A "product by process" claim is directed to the product per se, no matter how actually made, In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be

determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. Furthermore, Hshieh teaches a first insulative layer (120) that is thermally grown (column 3, lines 38-41 and column 6, lines 7-10).

Response to Arguments

2. Applicant's arguments with respect to claims 2-8, 10-14, 16, 18, 20 and 31 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however,

will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Edgardo Ortiz (Art Unit 2815), whose telephone number is (703) 308-6183 or by fax at (703) 308-7722. In case the Examiner can not be reached through a direct telephone call, you might call Supervisor Tom Thomas at (703) 308-2772. Any inquiry of a general nature or relating to the status of this application should be directed to the Group 2800 receptionist whose telephone number is (703) 308-0956.

EO/AU 2815

10/26/03

Tom Thomas

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